AMENDMENT(S) TO THE SPECIFICATION

Please replace paragraph [0004] with the following rewritten paragraph:

It is known that avalanche current may flow in such devices under reverse bias. This avalanche current flows into the ~~channel~~ body region and under the source regions of the MOSgated structures ~~(the R_b^+ region of the device)~~ (hereinafter referred to as "the under the source region" or "the under the source regions") and then to the source metal. If the horizontal portion of the avalanche current, hence, the voltage drop across the source - P body junction, is high enough, it can turn on the parasitic transistor in the MOS structure.

Please replace paragraph [0007] with the following rewritten paragraph:

In other words, to achieve both high breakdown voltage and high avalanche energy is a critical technique in the design of superjunction type of devices. When a superjunction device works with a perfect charge balance condition, it can support high reverse bias voltage. However, the large amount of the horizontal avalanche current through the [[R_b^1]] under the source region will easily trigger the bipolar structure in the MOSFET device. On the other hand, when the device works with a higher, and unbalanced p-charge in the pylons, avalanche energy is usually high, but with a low breakdown voltage.

Please replace paragraph [0009] with the following rewritten paragraph:

A device according to the invention produces a favorable trade-off of breakdown voltage and avalanche energy. When only the top of the pylon receives a higher dose implant relative to its lower portion, the device can still withstand a high breakdown voltage. When the device is avalanched, the avalanche current is uniform at the lower portion of the device and starts to converge toward each pylon when it flows close to the top of the device. This keeps the avalanche current away from the [[R_b^1]] under the source region so that the device can hold a much higher avalanche energy.

Please replace paragraph [0017] with the following rewritten paragraph:

A MOSgated structure is also provided in the usual manner, and is shown as P^- ~~channel~~ body regions 30, 31, 32 which receive N^+ source regions 33, 34, 35 respectively, which may be annular regions. The P^- regions in ~~channels~~ body regions 30, 31 and 32 which are below the sources ~~40, 41 and 42~~ 33, 34, and 35 respectively are the [[R_b']] under the source regions through which avalanche current can flow.

Please replace paragraph [0018] with the following rewritten paragraph:

A gate oxide 40 overlies the invertible channel regions between the source regions and ~~respective channel regions~~ N type body 23 and a polysilicon gate electrode 41 overlies the gate oxide 40. An insulation layer 42 such as LTO overlies and insulates the polysilicon gate segments of gate 41 from an overlying source electrode 43. A drain contact 50 is connected to the bottom of wafer 10.

Please replace paragraph [0023] with the following rewritten paragraph:

Thus, achieving both high breakdown voltage and high avalanche energy is the aim of the critical design of superjunction type of device. When a superjunction works at perfect charge balance condition, it can support high reverse bias voltage between electrode 43 and 50 (Figure 1). However, a large avalanche current through the [[R_b']] under the source region will easily trigger the bipolar structure in the MOSFET device section. On the other hand, when the device works with a higher p-charge in the pylon, avalanche energy is usually high, but with a reduced breakdown voltage.

Please replace paragraph [0024] with the following rewritten paragraph:

This invention improves the trade-off of breakdown voltage and avalanche energy. Thus, when only top of the p-column 20 receives a higher dose implant P_2 (than that of the lower portion of the p-column), the device still can withstand a relatively high breakdown voltage. When the device is avalanched, however, the avalanche current, as shown by arrows in Figure 3, is uniform at the lower portion of the device but starts to converge toward the p-column close to

top of the device. This keeps the avalanche current away from the [[R_b']] region under source 33 so that the device can handle a much higher avalanche energy.